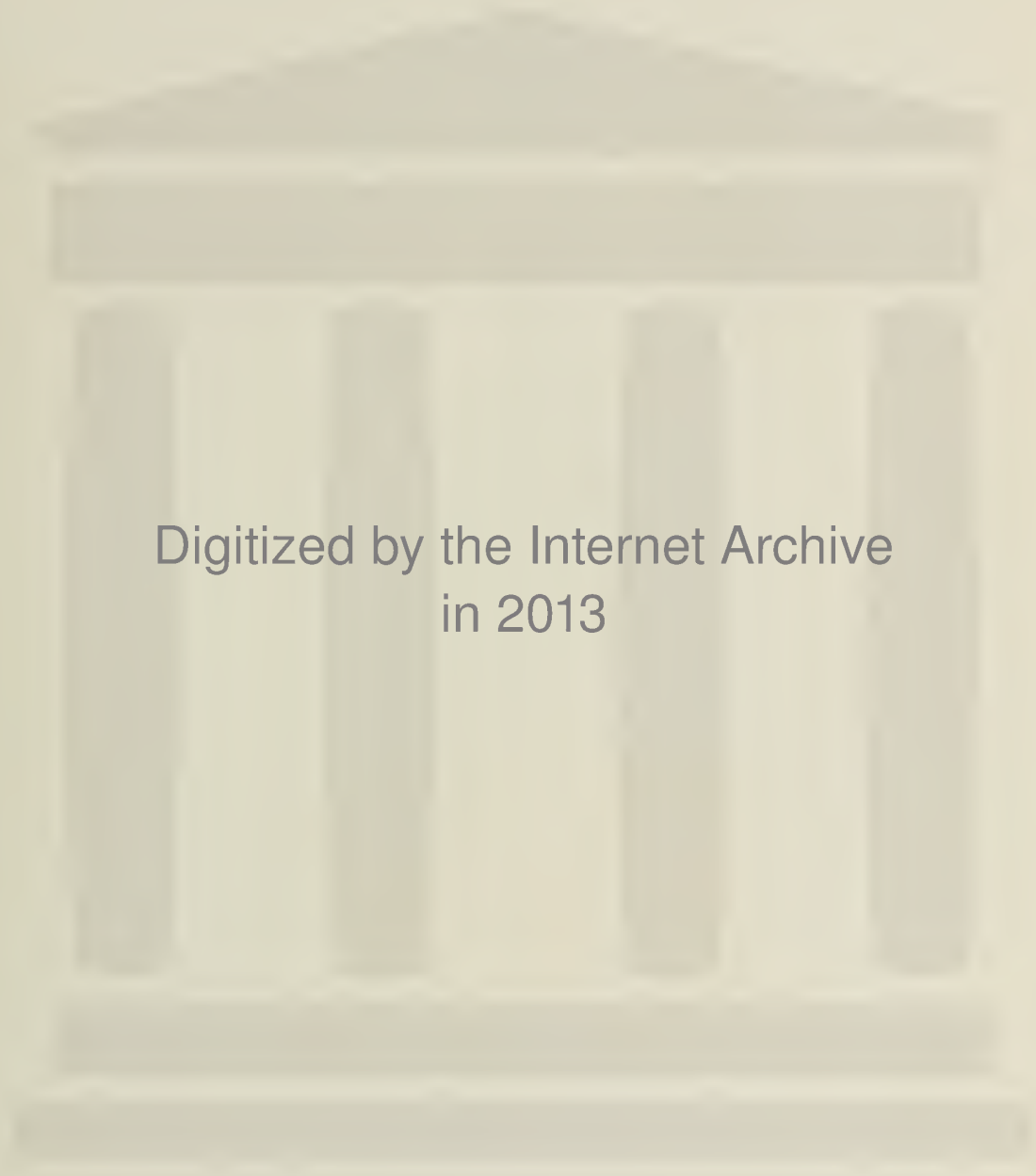

UNIVERSITY OF ILLINOIS
GRADUATE COLLEGE
DIGITAL COMPUTER LABORATORY

REPORT NO. 79

A ONE-WORD MODEL OF A WORD-ARRANGEMENT MEMORY

by

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A ONE-WORD MODEL OF A WORD-ARRANGEMENT MEMORY

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1. Word-Arrangement Memory

Introduction

The word-arrangement memory, first proposed by the Bureau of Standards,[1] may be made considerably faster than the conventional, core memory. There is no limitation on current selection ratio for the read-pulse, and a 3:1 selection ratio is possible for the write-pulse while the conventional memory is limited to a 2:1 ratio for both pulses (Notes on Magnetic Memories, File 218, May 14, 1957). This report deals with modifications of the word-arrangement memory, and describes experiments with a one-word model built to obtain answers to certain questions regarding the performance of these modified memories.

Two modes of operation have been considered, (1) with destructive sensing as in the conventional, core memory, and (2) with non-destructive sensing according to a method described in Section 4 of this report.

Description of Memory

A block diagram of the memory in the form using destructive sensing is given in Figure 1. The memory core-matrix consists of one column of cores for each word and two rows of cores for each bit. One wire, labelled W, runs through all cores of any one word. Three wires, perpendicular to this one, run through the cores representing the corresponding bit of all words. Only those for one bit are shown in the diagram. Two of these wires, labelled B_0 and B_1 are connected to bit-selection drivers, and the third labelled S is connected to the sensing amplifier. All three wires thread both cores of each bit in series opposition.

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1. NBS Report October 1954 - March 1955 Progress on Computer Components.

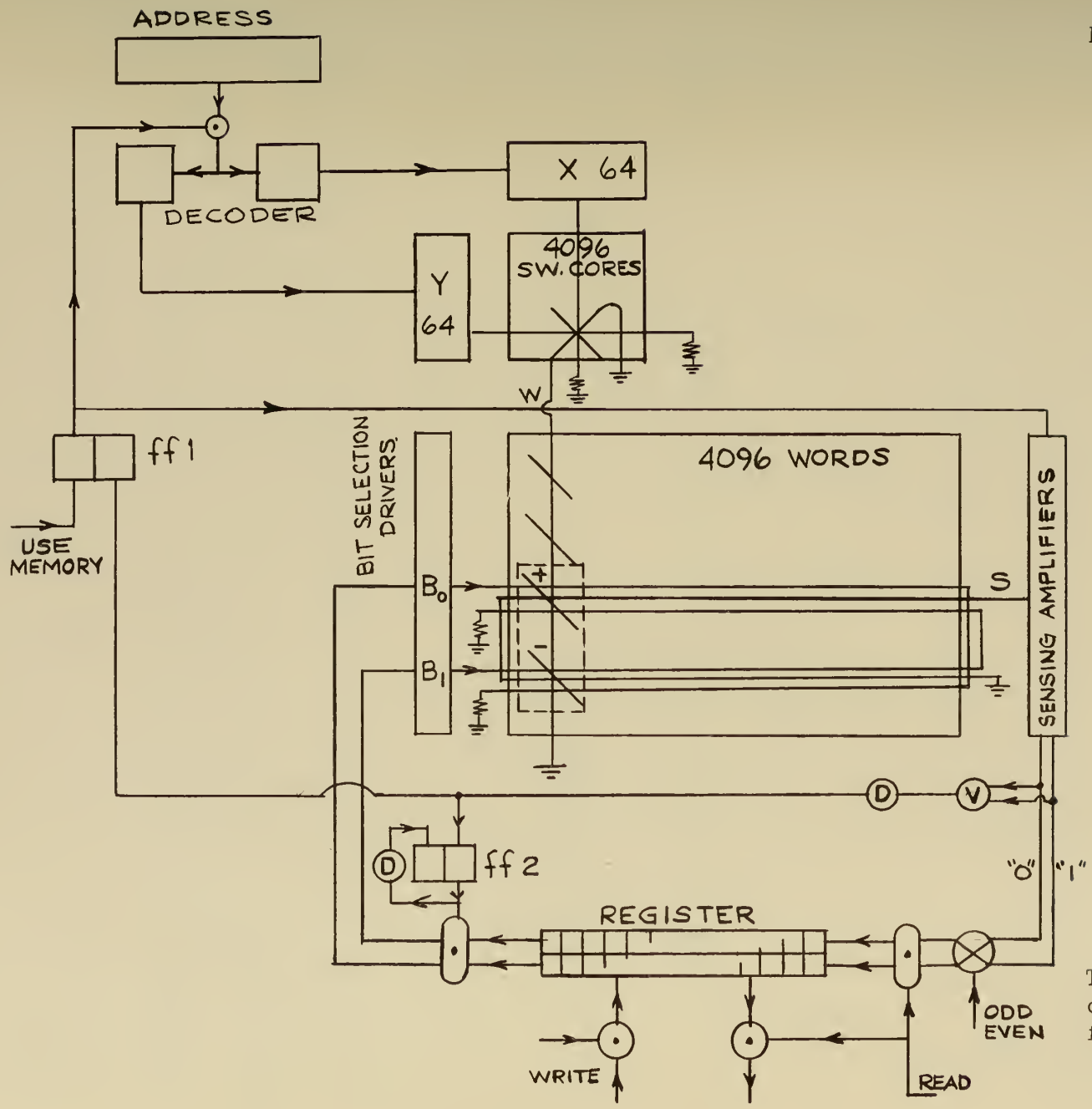

Figure 1. Word-Arrangement Memory

Transpose "0" and "1" for even, odd addresses to avoid pick-up from B pulses.

The other parts of the memory need not be described here as their nature is indicated by their functions as outlined in the following paragraphs.

Operation of Memory

Since the sensing process is destructive it must be followed by a rewrite process. Two steps are also required to store information in the memory, a clear process and a write process. Thus both sensing and storing require a similar sequence of operations. This sequence is described in the next paragraph.

A signal initiating a memory cycle sets ffl, allowing the address to be gated through the decoder to the X and Y drivers. The Y drivers are normally conducting so that all the switch cores are biassed in a given direction. When the signal from the decoder reaches the drivers the selected Y driver is turned off and the selected X driver is turned on (See Figure 2).

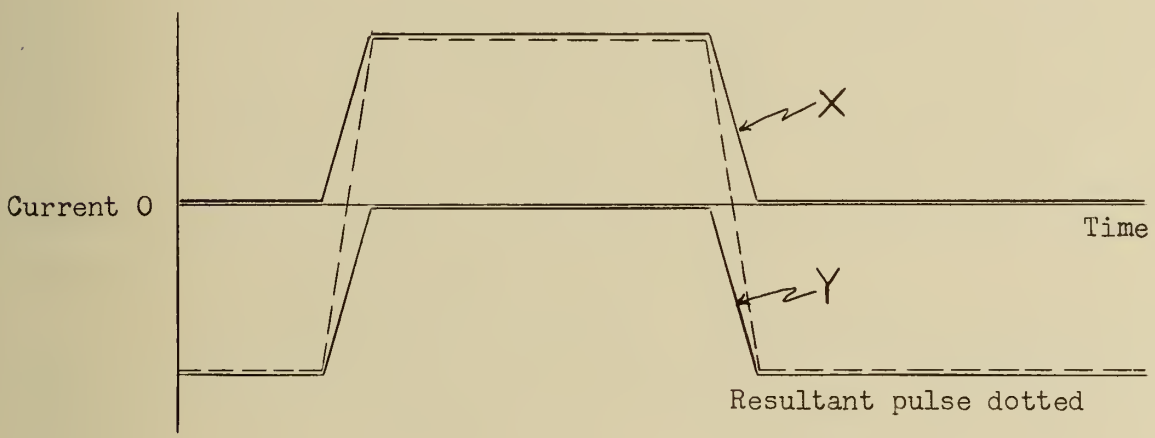

Figure 2. X, Y Pulses.

Only the selected switch core operates, producing an output through the W wire with the wave form shown in Figure 3.

The two cores representing one bit of one word, for example those shown in the dotted rectangle in Figure 1, are normally in opposite states of magnetization. The pulse in the W wire brings whichever core was in the minus

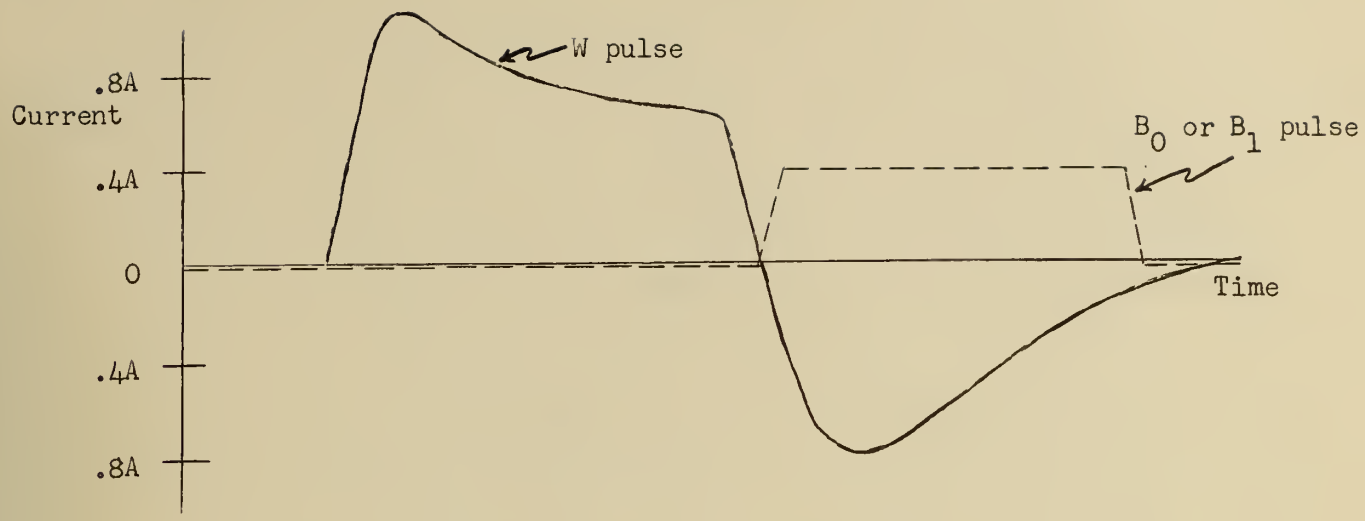

Figure 3. W pulse and B pulses.

state to the plus state. As a result a pulse is produced in the sensing wires threading these cores. Whether the bit stored was a "1" or a "0" will determine whether the output pulse is positive or negative. The fact that a pulse is produced in either case may turn out to be useful in checking circuits. Output pulses for a "0" and a "1" are shown in Figure 4. Due to a strobe pulse from ff1, the sensing amplifier is active only during the first part of the cycle corresponding to the full lines in the diagram.

The sensing amplifier produces a signal on one or other of two output lines (for each bit) and sets the corresponding bit of the register in the appropriate sense. The output of the sensing amplifier also sets ff2 and resets ff1, turning on either B_0 or B_1 for each digit and returning the X and Y drivers to their normal states. The switch core is driven back to its normal state producing a reverse pulse (second half of Figure 3) which is aided by the B driver in one core and opposed in the other. Thus only one core of the pair is switched. Which core is switched will depend on the setting of the register. For a sensing cycle the register will contain the word which has been read from the memory. For a storage cycle the register will contain the word to be stored.

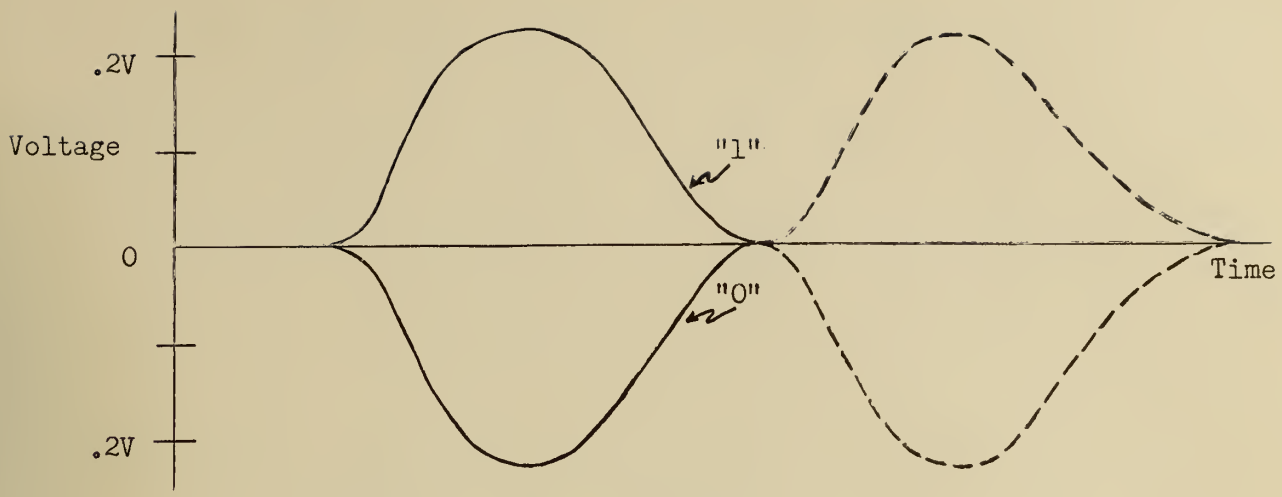

Figure 4. Signal outputs.

The X and Y lines through the switch cores and the B_0 and B_1 lines through the memory cores form transmission lines or low-pass filters, and must be terminated correctly to avoid reflections. The W lines, on the other hand, pass through relatively few cores, the same number of which are switched on each cycle no matter what word is stored. Therefore the load on the switch cores is almost purely resistive and does not vary from one cycle to another, although it does vary with time during each cycle. No external resistance is needed to terminate the W lines. This reduces the power which must be supplied by the switch cores. It also means that the total flux change in the memory cores of a word is very nearly equal to the flux change in the switch core, since the resistance of the W wire is quite small.

Partial Switching

In most memory applications the cores are completely switched from one remanent state to the other. This is not necessary when compensating cores are used since reversible flux changes in the two cores concel out and a good signal-to-noise ratio may be obtained even when the cores are only partly switched.

The two hysterisis loops in Figure 5 represent the two cores of a given bit. Suppose core a is in state A and core b in state B. The read-pulse brings

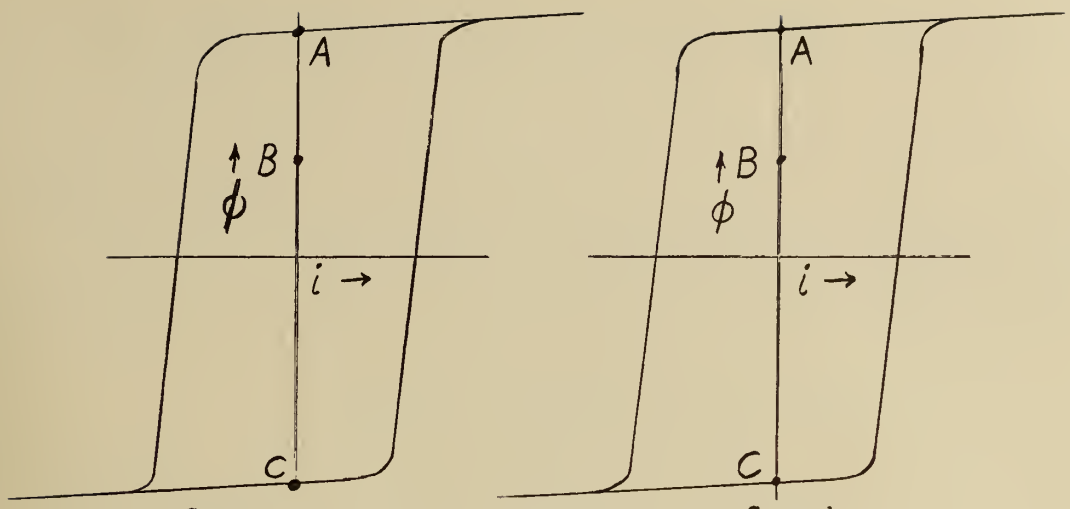

Figure 5.

core b into state A also. During the write-pulse either core a or b will be brought to state B, the amount of flux change being limited by the available flux change of the switch core.

Partial switching would have two advantages. It would reduce the power dissipated in the memory cores making the problem of heating less serious, and it would reduce the size of the switch cores and the power required to drive them. Unfortunately it would not reduce the value of the current required.

2. One-Word Model

Purpose

Some parts of the operation of the memory described in Section 1, such as the action of the switch cores, and the size of the B pulses which can be safely used without disturbing cores of unselected words, can be predicted with some confidence. On the other hand only rough estimates can be made of switching time, current regulation in the W pulses, best size of switch cores, etc. The one-word memory was constructed as the simplest arrangement which would give any experimental data regarding these questions.

The actual amplifiers used were made in the most convenient way from the point of view of a laboratory model. They are not intended to be prototypes. The use of secondary-emission tubes might not be desirable in a full-scale memory.

Also some feed-back would have to be provided to maintain current tolerances. This problem is considered further in Section 5.

Description

Figure 6 is a block diagram of the one-word model. Circuit diagrams of the various parts are given in Figures 7 - 11. Table I lists the specifications of these units.

Table I. Equipment Specifications

Core Plane: 100 S-1 cores diameter 0.08"

Switch core: 24 S-3 cores
nominal
(changed during tests)
4 turns input
4 " bias
1 or 2 " output

Switch core Driver: Output: 0.3 - 1.5 Amp. adjustable

Rise time: 50 mμ sec.
Delay: 75 mμ sec.
Input: +6v. pulse (91 ohms)
Duty cycle: 10%

Inhibit (B) Driver: Output 0.2 - 0.5 Amp. adjustable

Rise time: 50 mμ sec.
Delay: 75 mμ sec.
Input: +6v pulse
Duty cycle: 10%

Clock: Output: 6v (91 ohms)

Rise Time: 25 mμ sec.
Pulse length: adjustable .1 - 1.0 μ sec.
Duty cycle: 10%

Sense Amplifier: Amplification: $\sim$ 200

Delay: 50 mμ sec.
Rise Time: 150 mμ sec.

Register: Output: 0 or -20 v.

Switching time: 100 mμ sec.
Delay: 50 mμ sec.

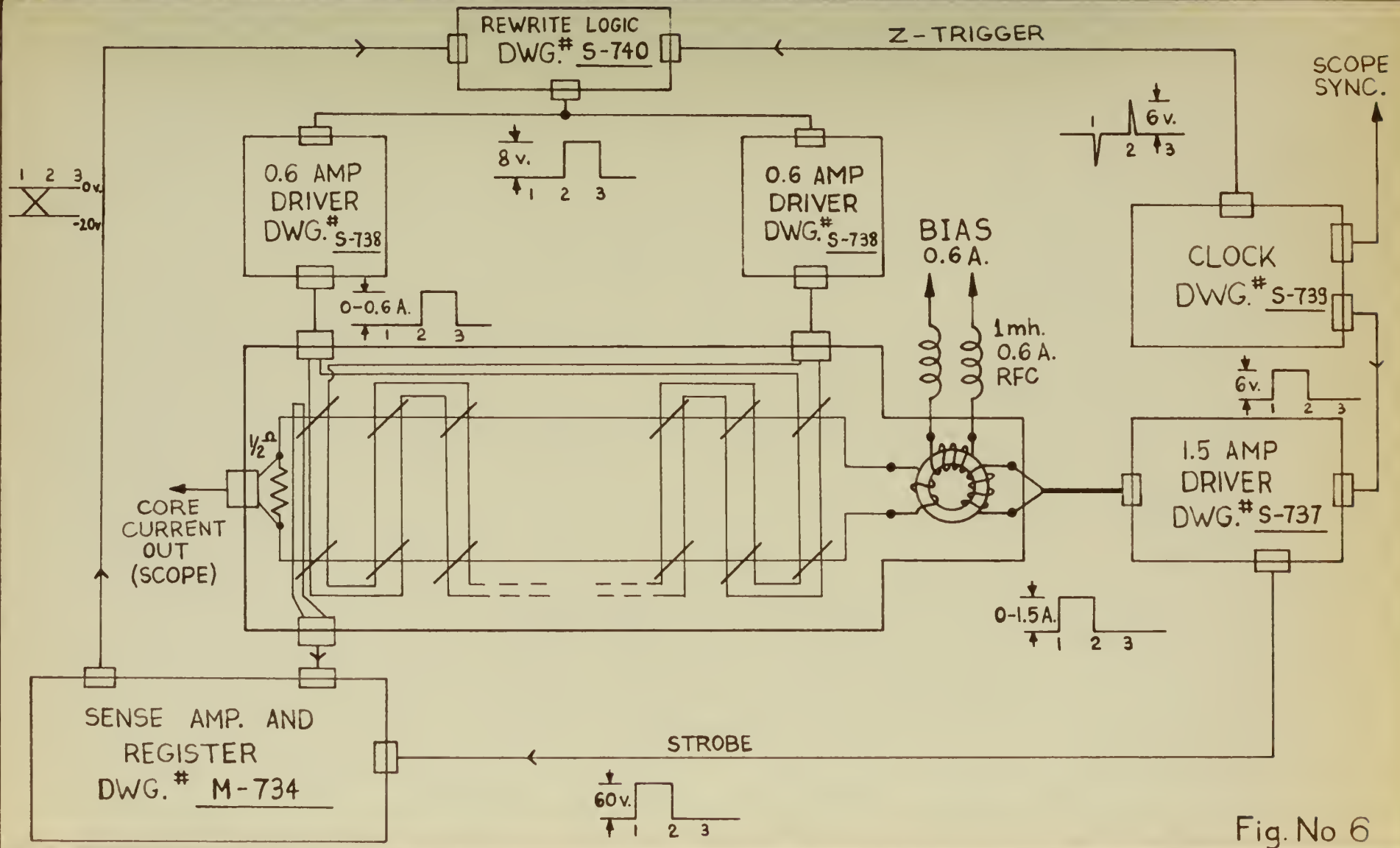

Fig. No 6

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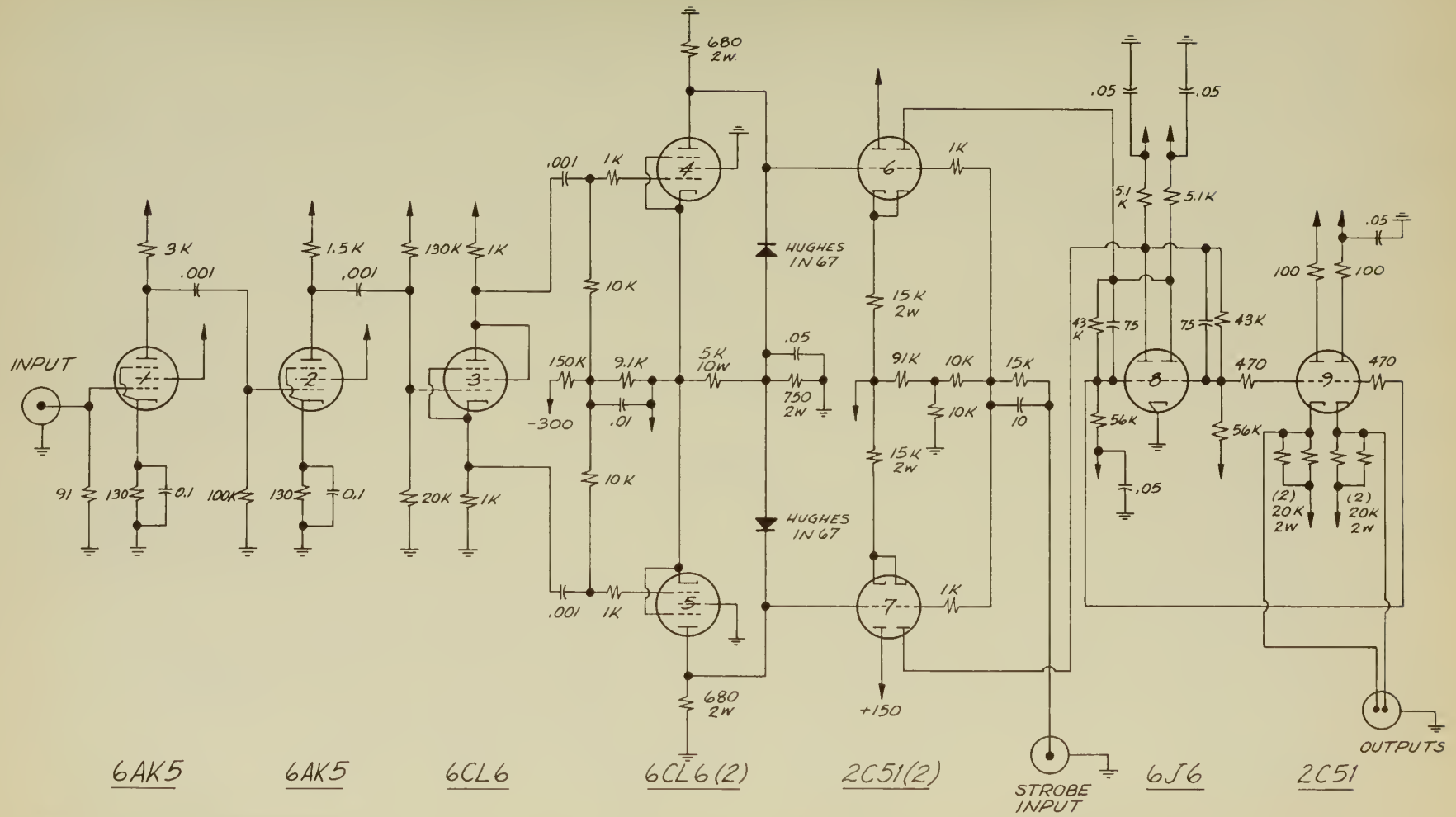
FOR C.P. BY B.S. CHECKED Christopher Pettle APPROVED R. E. Meagher DATE 5-3-57

TITLE — ONE-WORD CORE MEMORY

S-736



UNLESS OTHERWISE SPECIFIED:
ALL UP VOLTAGES ARE +150 V.
ALL DOWN VOLTAGES ARE −150 V.
ALL RESISTORS ARE ½ W.
ALL FILAMENTS ARE GROUND EXCEPT 4 & 5 WHICH ARE PEGGED AT −150 V.

Fig. No 7

UNIVERSITY of ILLINOIS — GRADUATE COLLEGE — DIGITAL COMPUTER
FOR H.NY BY DAW CHECKED H.N.Yu APPROVED R. J. Mangano DATE 4-29-57
TITLE — SENSING AMPLIFIER & REGISTER

M734

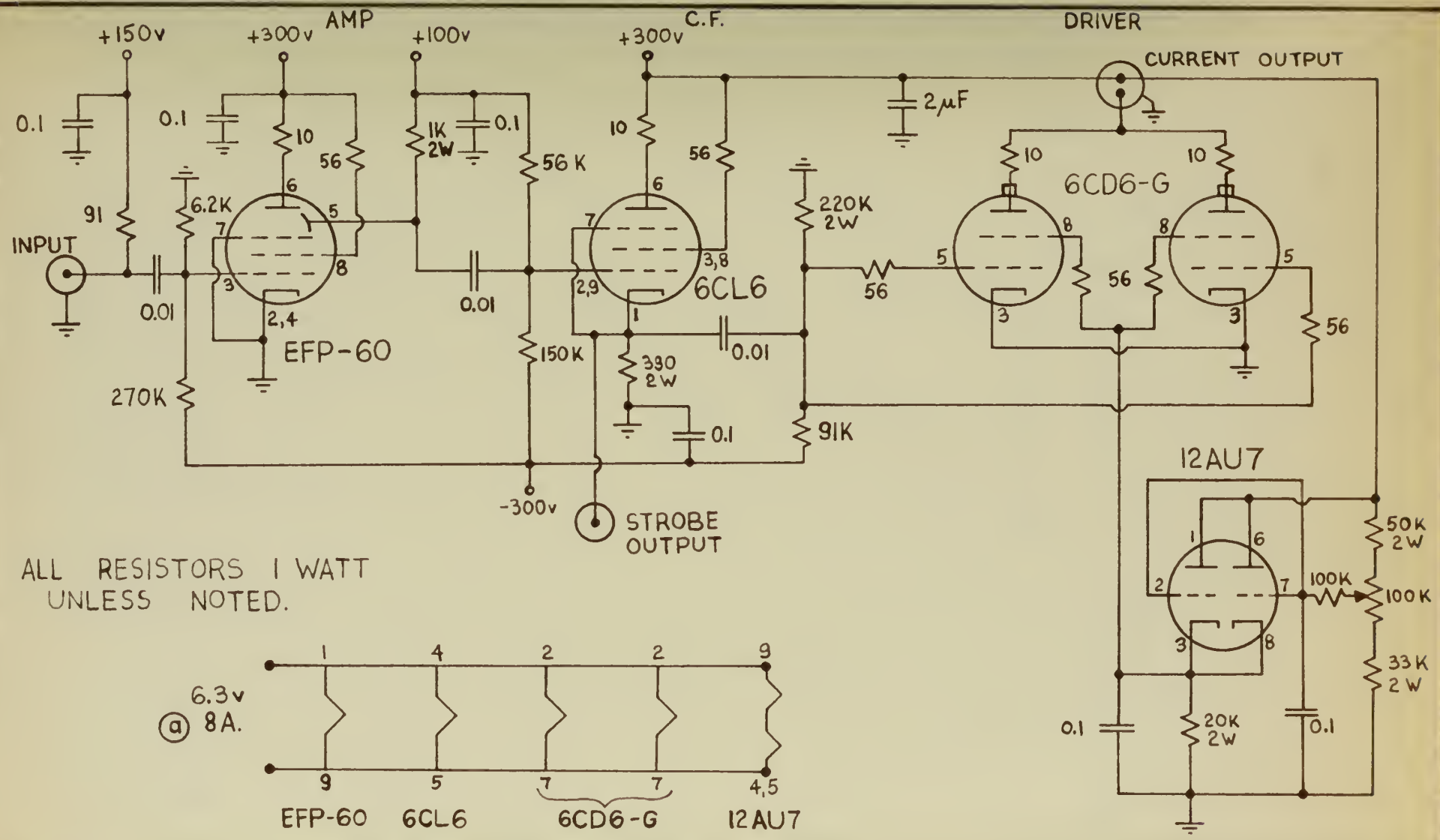


Fig. No 8

UNIVERSITY of ILLINOIS — GRADUATE COLLEGE — DIGITAL COMPUTER

FOR C.P. BY B.S. CHECKED Christopher Pottle APPROVED R.E. Meagher DATE 5-6-57

TITLE — 1.5 AMP. MAGNETIC CORE DRIVER

S-737

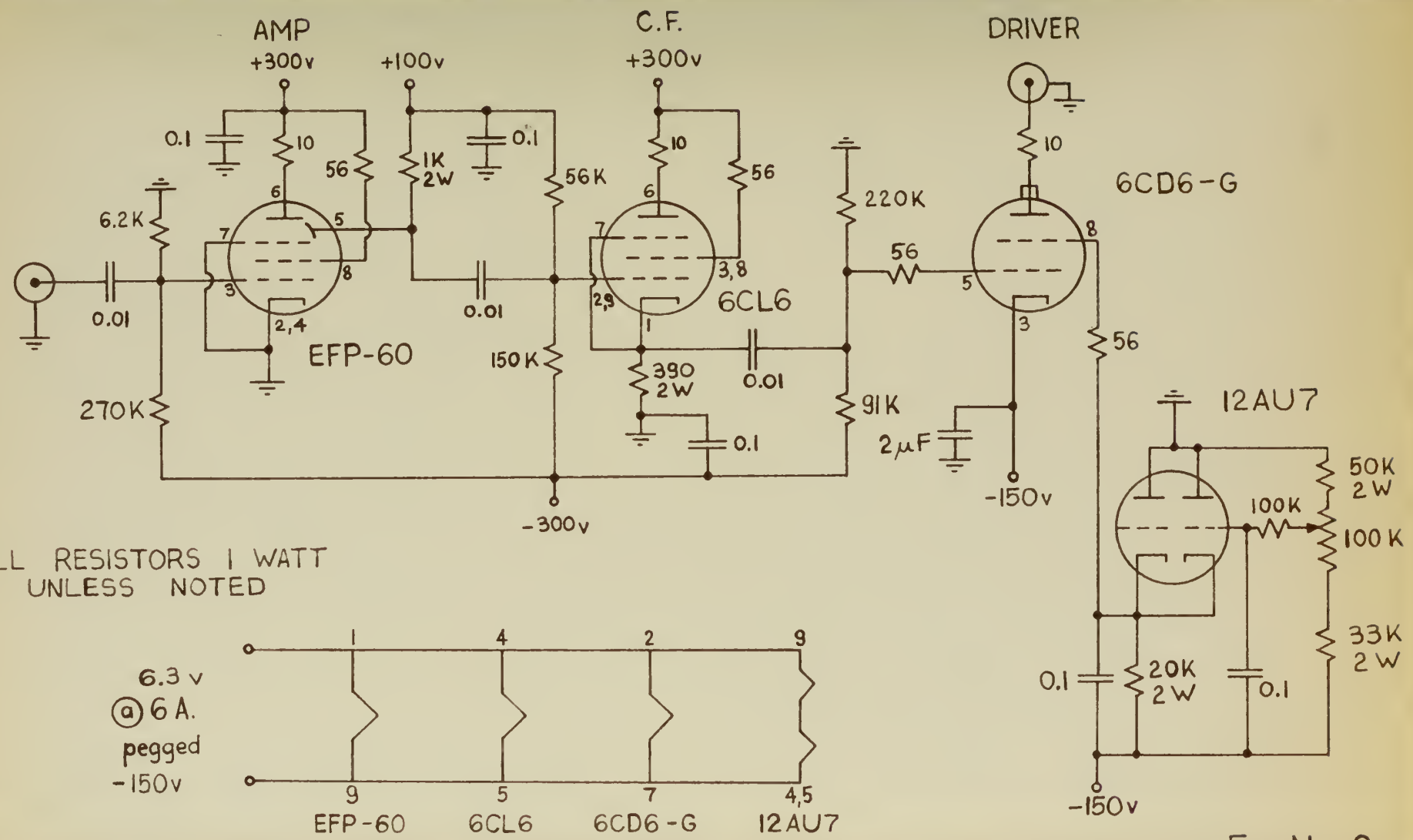


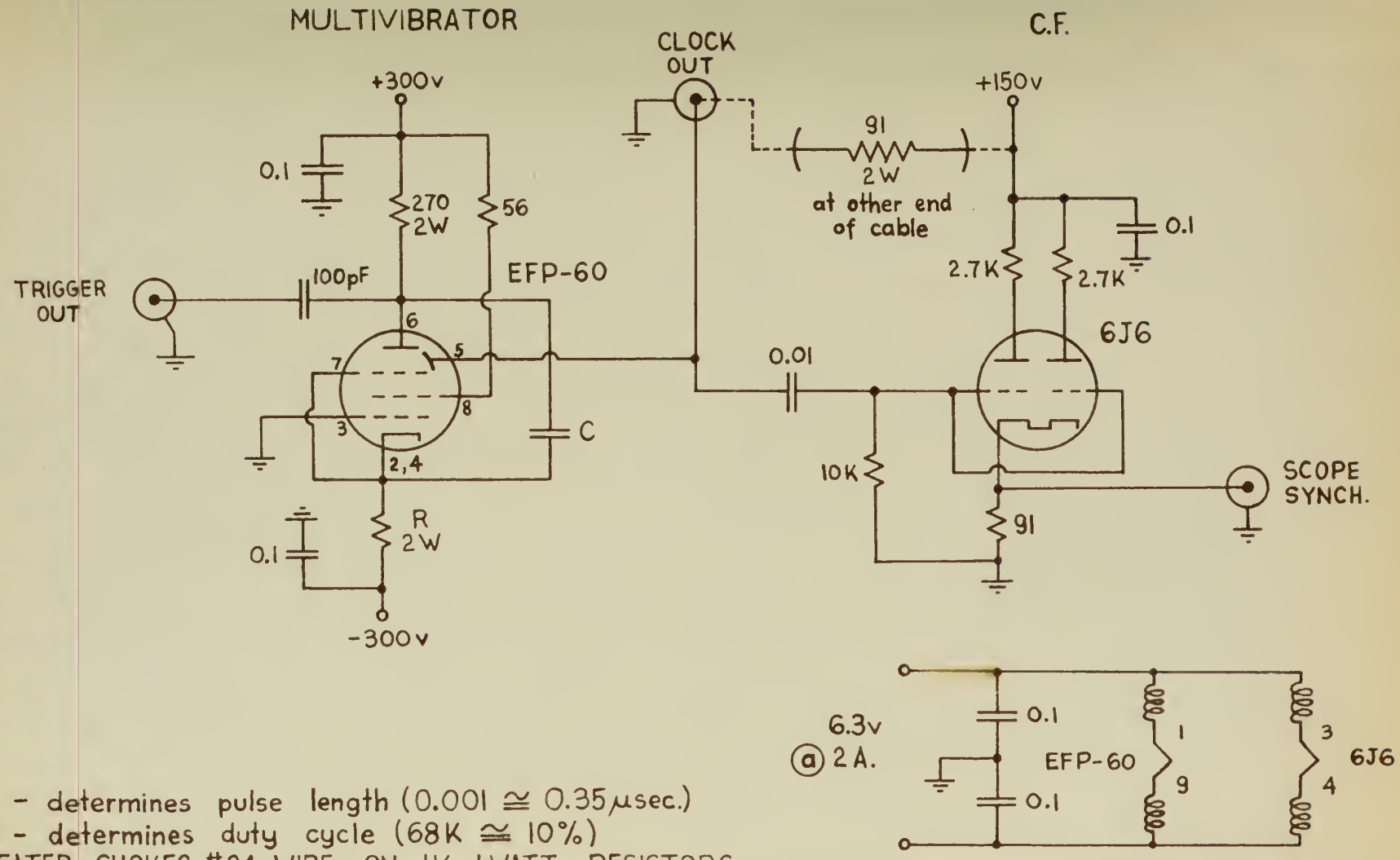
Fig. No 9

UNIVERSITY of ILLINOIS — GRADUATE COLLEGE — DIGITAL COMPUTER

FOR C.P. BY B.S. CHECKED Christopher Pottle APPROVED K.E. Meagher DATE 5-8-57

TITLE — 0.6 AMP. MAGNETIC CORE DRIVER

S-738



C - determines pulse length (0.001 ≅ 0.35 μsec.)
R - determines duty cycle (68K ≅ 10%)
HEATER CHOKES #24 WIRE ON 1K 1 WATT RESISTORS
ALL RESISTORS 1 WATT UNLESS OTHERWISE NOTED.

Fig. No 10

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FOR C.P. BY B.S. CHECKED Christopher Pottle APPROVED R. E. Meagher DATE 5-9-57

TITLE — CLOCK - ONE WORD CORE MEMORY

S-739

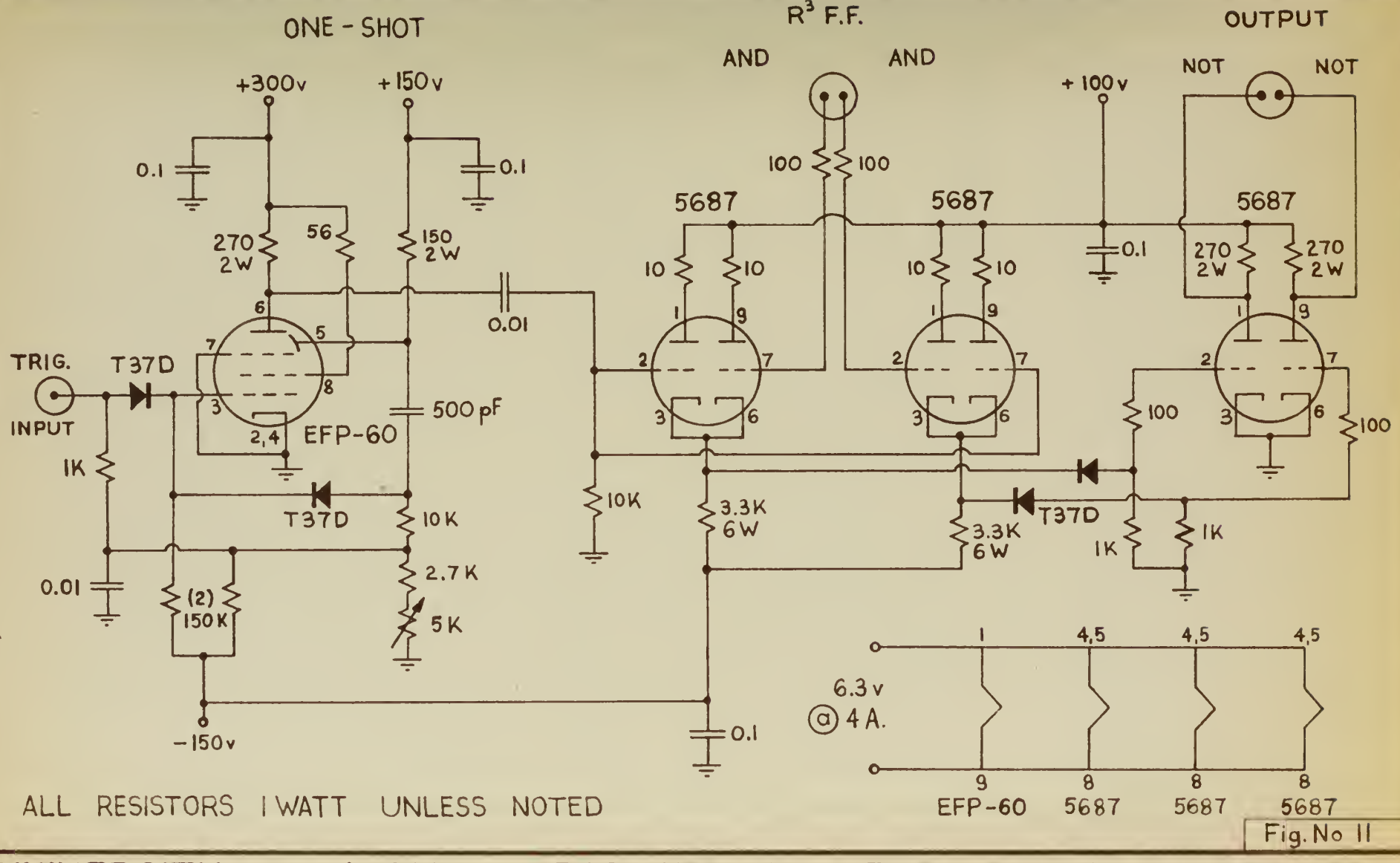

Fig. No 11

UNIVERSITY of ILLINOIS — GRADUATE COLLEGE — DIGITAL COMPUTER

FOR C.P. BY B.S. CHECKED Christopher Pattle APPROVED R.E. Meagher DATE 5-11-57

TITLE — REWRITE LOGIC — ONE WORD CORE MEMORY

S-740

The memory consists of 100 cores (Type S1) strung on drive wires so that each pair of cores represents one bit of a 50-bit word. However, as only two bit-selecting amplifiers were constructed these 50 bits cannot be selected independently. Only two combinations, 1010 ....10 and 0101....01, can be selected. Several operations are possible, reading and writing either word repeatedly, reading one word and writing the other alternately, or several simple sequences controlled by a counter. These operations should be sufficient to determine whether or not the first few cycles following a change in word stored are appreciably different from steady-state cycles.

Current Specifications

Certain limits are placed on the values of current pulses by the fact that the model is intended to represent part of a larger memory.

1) Bit-selection pulses must not exceed the value of I/2 for S_1 cores (0.42 amp) so that cores of unselected words would not be affected.

2) The output pulse from the switch cores on the write part of the cycle should not exceed the value of the bit-selection pulse plus I/2. This condition need not be exactly met since the pulse is applied only to cores of the selected word, and a small change in the core which is supposed to be held fixed does not matter as long as the other core changes much more.

3) If the X and Y drivers are to be simple on-off switches the X pulse must not exceed the Y pulse by more than i_o for the switch core.

Choice of Switch Cores

A switch core may be a very inefficient pulse transformer because the energy required to reverse the magnetization of the core itself may exceed the energy output. It is readily shown that the energy lost in the switch core is least when the radius is least. However the area of cross section must be great enough to supply the required flux change. Therefore long narrow cylinders would be ideal switch cores. A more practical arrangement having the same desirable features is provided by a switch made up of a number of 0.08 inch ferrite cores strung together. The heating effects should also be small in such a switch because of the large surface-to-volume ratio.

Switches made up of small ferrite cores in this way have been used in most of the tests on the one-word model. A few tests were made using permalloy ribbon cores.

3. Experimental Results

Preliminary Tests

Much of the preliminary testing need not be described, as anything useful in the results is included in the description of later experiments. However some comparisons of permalloy and ferrite switch cores made before the model was complete have not been repeated and are therefore briefly summarized here.

1) Ferrite cores seemed to be preferable to permalloy cores for switches with the type of load provided by the W-lines in this model, because damped oscillation or "ringing" was produced by the permalloy cores. This effect could be eliminated to a large extent by damping resistances but at the cost of considerable wasted power.

2) Because the diameter of available permalloy cores was larger than the .08 inch ferrite cores the power loss in permalloy cores was greater. Also their inductance was greater which would lead to a longer transmission time through the 64x64 array.

3) The larger coercive force of the ferrites may also be useful since it allows the current used for producing the read pulse to be larger than the bias which produces the write-pulse. Only the write-pulse is fixed by the 3:1 ratio, so that any increase of the read-pulse relative to the write-pulse helps to reduce the time for the read cycle.

Normal Operation

In the model which has been described, tests were made using a switch composed of 24 ferrite cores with 4-turn primary windings and a 2-turn output winding. When these cores are switched the change in flux through the 2-turn winding should be sufficient to completely reverse the magnetization of the 50 memory cores through the single turn W winding.

Some typical wave forms are shown in Figure 12 and Figure 13. In Figure 13 four wave forms are superimposed, corresponding to the four steps of the following sequence.

(1) read "1" write "0"
(2) read "0" write "0"
(3) read "0" write "1"
(4) read "1" write "1"

It will be noticed that the signal is slightly different when a "1" is read following a "1" than when the previous signal was a "0". The effect is not cumulative and a continuous sequence of 1's gives only a slightly different result.

The complete cycle of operation in the model takes 0.8 μ sec. However, in a full-scale memory, time for decoding and for transmission of pulses through the core matrix together with tolerances would increase the total time to about 1.5 μ sec.

Partial Switching

In the last part of Section 1, we discussed the advantages of limiting the flux change in the memory cores to less than the full swing from one remanent point to the other. The tests described below indicate that this procedure is quite possible although the range of conditions over which it operates successfully is somewhat narrower than for complete switching.

Operation in this mode is slightly faster than the "normal" operation and as a result some difficulty was experienced due to delays in the sensing amplifier. When a transistor version of the sensing amplifier has been made these delays can be decreased. In the meantime tests were made with a modified circuit in which the changes from 1010....10 to its complement were controlled by a counter instead of by the output of the amplifier.

Partial switching was obtained by decreasing the number of cores making up the switch, or by decreasing the number of output turns of the switch-core output winding from two to one. The form of the signal output curves are shown in Figure 14.

In Figure 15 is shown the effect of decreasing the length of the read pulse. The operation is nearly unchanged for decreases in pulse length down to .4μsec, below which the amount of switching decreases rather suddenly. The pulse-length which corresponds to this sudden change varies rather widely depending on other conditions.

Whenever the signals for "1" and "0" differ only in sign, and the magnitude of signals for various sequences of 1's and 0's are nearly the same, we can be reasonably sure that the model is operating correctly as described in the last part of Section 1. For excessively long or short pulses the model does not operate correctly, as shown by this criterion. It is very difficult to show experimentally exactly how the system fails and also it is not possible to predict theoretically for what conditions failure might be expected.

The difficulty in showing experimentally what is happening when the system fails is due to the fact that no convenient means exists for finding out the state of magnetization, ϕ, of a core at any instant.* The output voltage from the core is a measure of $\frac{d\phi}{dt}$, and cumulative errors in integrating this signal, particularly over a number of cycles, make it difficult to use the signal to measure the instantaneous values of ϕ.

As regards theoretical prediction, a complete statement of the difficulties in dealing with cores linked together by a low-resistance loop would be long and unprofitable. It may be sufficient to point out the change in flux of the switch core and the net changes in flux of the memory cores are related by the equation

$$\phi_{\text{switch core}} = \phi_{\text{memory cores}} + R\int i\,dt$$

in which the small term $R\int i\,dt$ cannot be calculated exactly. (R is the small resistance of the wire linking switch and memory cores.) Although this term is small for a single cycle its effect over many cycles may be important. Under

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* A possible tool for determining the state, ϕ, of a core without altering it may be provided by the reversible response to small current pulses. It is shown in Section 4 that this response varies with the state of the core.

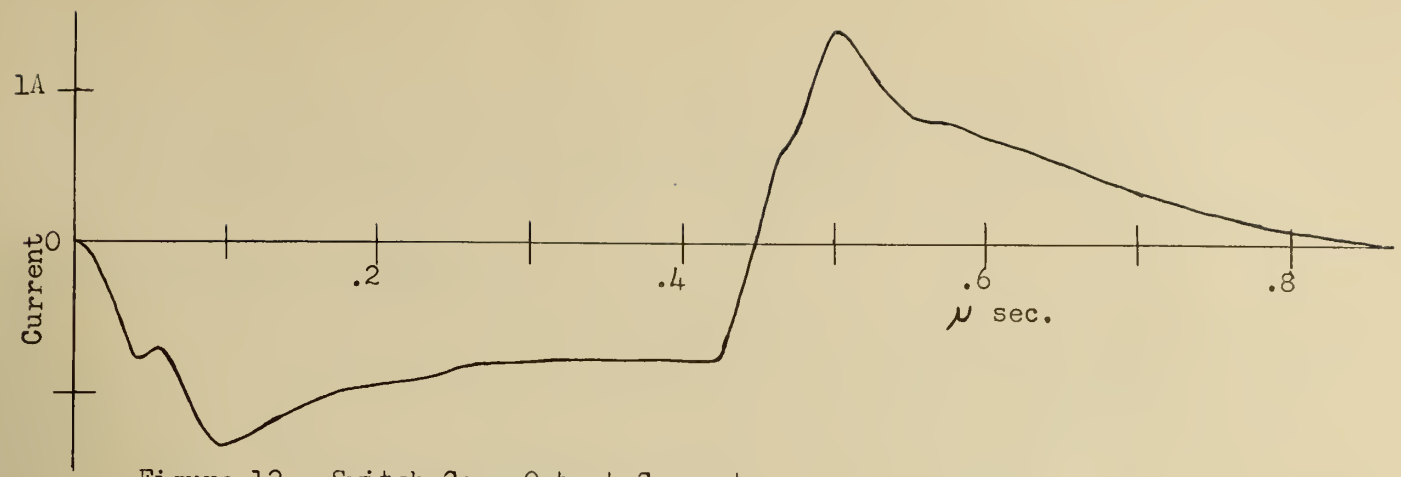

Figure 12. Switch Core Output Current

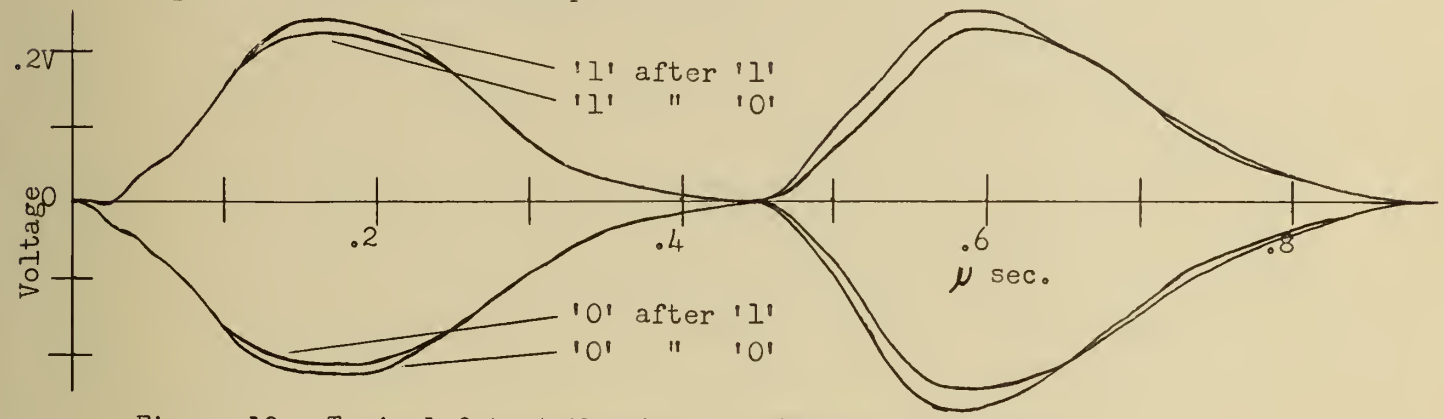

Figure 13. Typical Output Waveform for "Normal" Operation

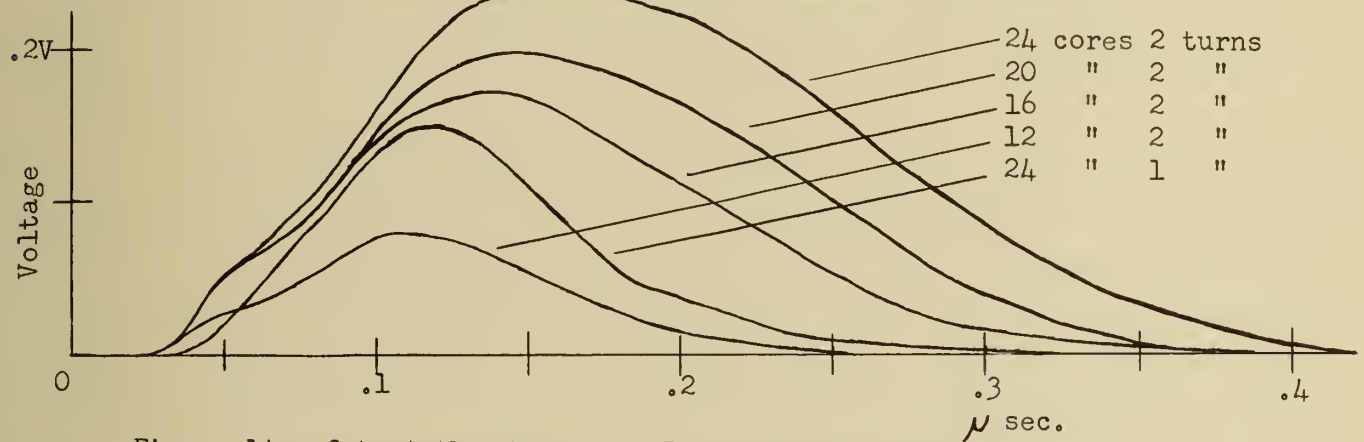

Figure 14. Output Waveforms for Partial Switching

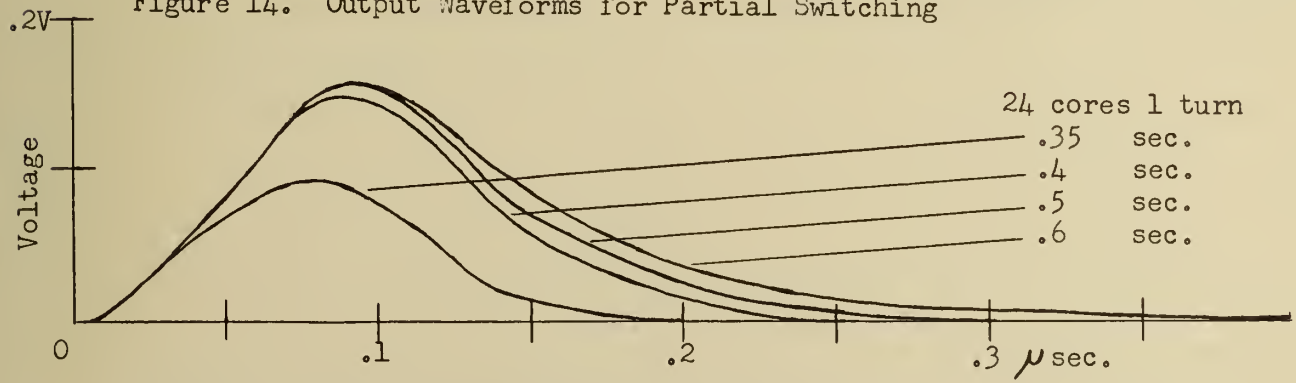

Figure 15. Effect of Duration of Read Pulse on Output Voltage

conditions of correct operation $\int i dt$ equals zero, but it is not possible to predict what arrangements will produce this condition.

4. Non-destructive Sensing

A possibility of non-destructive sensing arises from the fact that one of the cores representing a given bit may be only partially magnetized (or even practically demagnetized) whereas the other is completely magnetized. The slopes of the reversible magnetization curves for cores in these two states differ considerably. If the slope of the flux-current curve for the nearly saturated core is represented by L henries and that of the partially magnetized core by L' henries, the output voltage from the pair of cores when a current pulse passes through is $\pm(L'-L)\frac{di}{dt}$, where the sign depends on whether a "0" or "1" is stored. Provided the pulse is less than 0.4 amperes no permanent change in the state of the cores would occur. Some preliminary tests indicate that $\frac{L'}{L}$ is approximately 1.9 and that this ratio is almost independent of current so that comparatively small currents could be used.

Previous methods of non-destructive sensing have been based on the curvature of the hysteresis loop at the remanent point which provides a small difference even for quite large currents and a negligible difference for small currents.

One difficulty regarding the application of the idea of non-destructive sensing described in this report is that it is improbable that the small, fast pulses required could be handled by the switch-core array. Separate selection systems would be needed for the read and write pulses. One possible arrangement is shown in Figure 16. Provided the transformers T_{jk} had a secondary inductance not greater than 10^{-6} henries their presence would not affect the action of the write circuits. No tests have been made yet to determine whether air-core or ferrite-core transformers would be suitable.

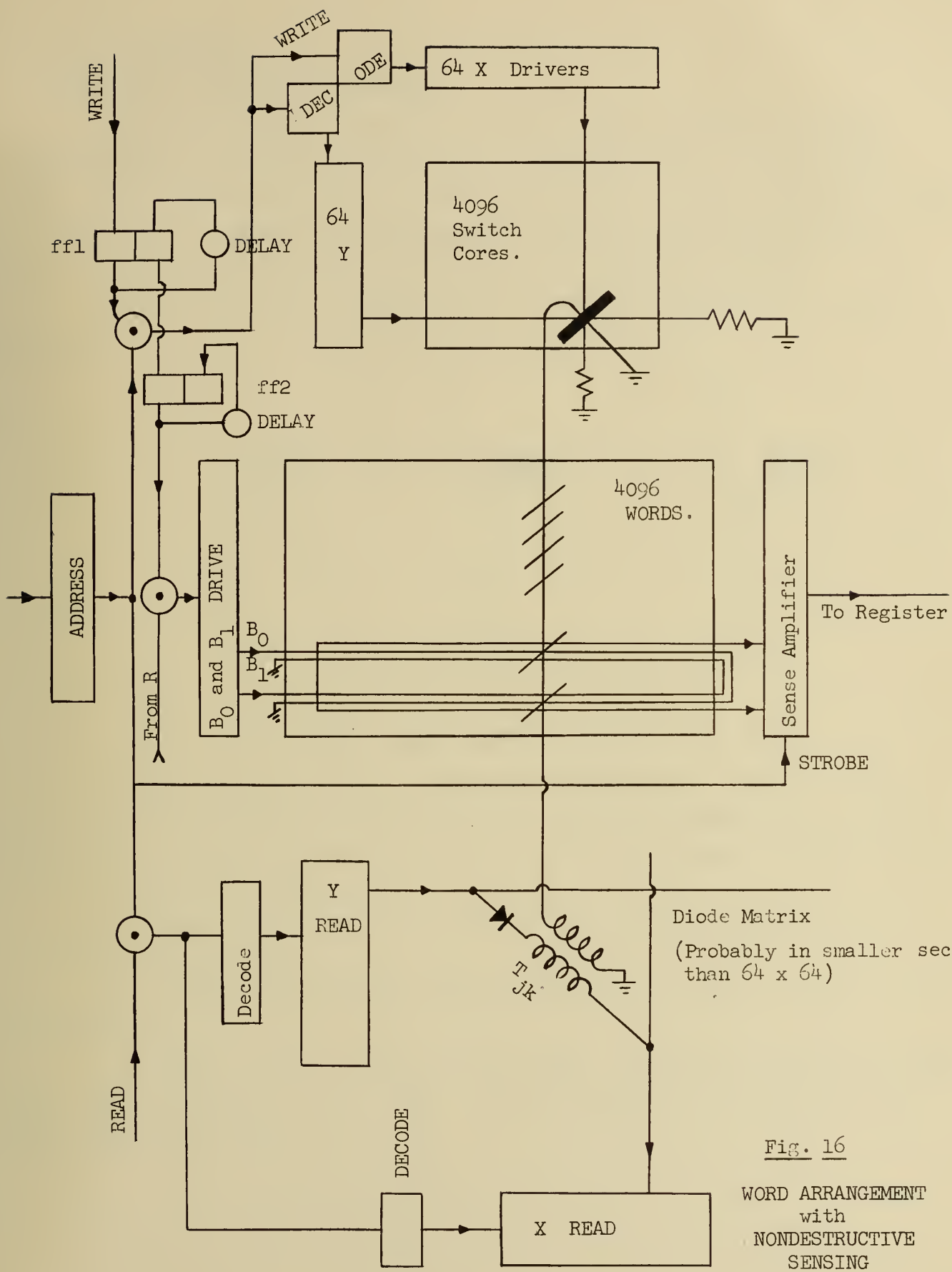

Fig. 16

WORD ARRANGEMENT
with
NONDESTRUCTIVE
SENSING

5. Other Experiments

Transmission Time in Switch Cores

While estimates are available for the transmission time for pulses through memory cores none are available for the switch cores. In a 4096 word memory X and Y pulses would have to travel through up to 64 cores. The actual time could only be determined after the geometry of the switch core array has been fixed, but an approximation has been made by the following experiment.

Eight switches each consisting of 24 ferrite cores with 4 turn X and Y windings and a 2 turn output winding were arranged as in Figure 17.

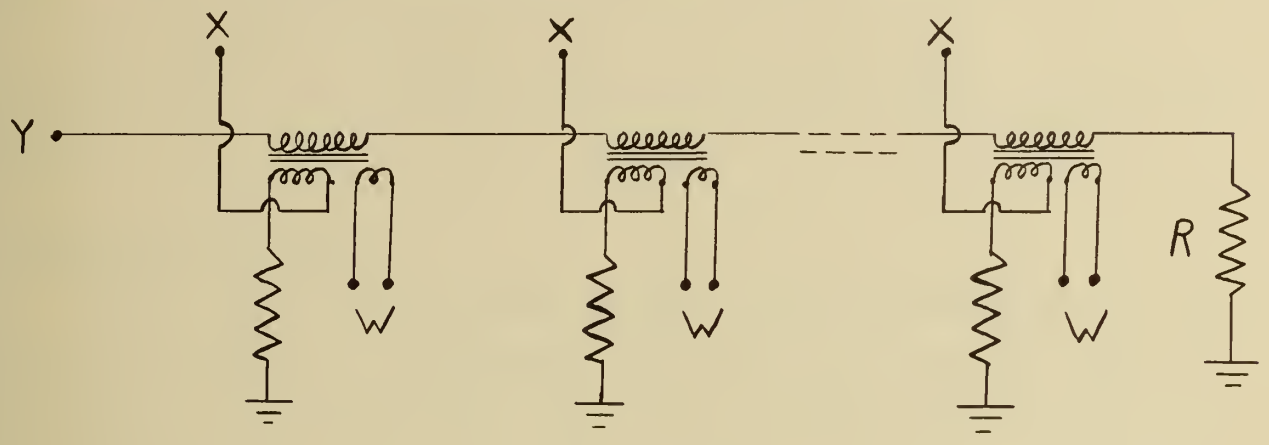

Figure 17. Switch Core Transmission Time Tests.

As can be seen the eight Y windings are connected in series. A pulse was fed into the Y winding at the left and a terminating resistor R, was provided at the right. Outputs from the first and last switch were compared on the oscilloscope, with the following results.

1) When both terminals of the X windings were open the delay through 8 switches was 6 mμ sec.

2) When each X winding was grounded through a resistor as shown the delay was 20 mμ sec.

The actual value in a switch matrix might be expected to lie between these values but rather nearer to the second. A safe estimate of the delay might be 2 to 3 mμsec per switch.

The terminating resistance used was 150 ohms, selected by trial and error.

As a check, the impedance and propagation constant of the line formed by the switch cores was calculated from measured inductance and capacitance of the switches.

$$L = 0.7\ \mu h$$

$$C = 12\ \mu\mu f$$

$$\text{Time} = \sqrt{LC} = 2.9\ m\mu \text{ seconds}$$

$$Ro = \sqrt{L/C} = 240 \text{ ohms.}$$

It can be seen that these value agree roughly with the values determined by direct measurement.

Bit-Selection Drivers

The bit-selection drivers must produce a pulse not exceeding 0.42 amperes into a load consisting of cores forming a transmission line of approximately 150 ohms impedance. The rise time should be as short as possible and the value of the current should be kept within narrow limits. Because the desired rise time of the pulse approaches the fastest possible with tubes the feed-back loop used to produce stability must be fairly simple. Not much time has been spent so far on developing a prototype driver, and none of the circuits so far studied appear to be entirely suitable.

6. Conclusions

The work described in this report was intended as a preliminary survey. The possibility of building a full-scale memory along the lines suggested in this report remains to be checked by tests on a larger model. However, as far as these limited tests go, the results are encouraging and indicate the desirability of a more extended test on a word-arrangement memory with compensating cores and small, ferrite switch-cores. Such a memory should have an access time about 1.5 μsec. If the further ideas of partial switching and non-destructive sensing can also

be incorporated. A memory with write-time 1.5 μ sec and read-time of a few tenths of a microsecond would result. The problem of heat dissipation would be comparatively slight in such a memory.